Exhibit 36

Library of Parameterized Hardware Modules for Floating-Point Arithmetic with An Example Application

A Thesis Presented

by

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Chapter 1

Introduction

Many image and signal processing applications benefit from acceleration with reconfigurable hardware. This acceleration results from the exploitation of fine-grained parallelism available in reconfigurable hardware. Custom circuits built for these applications in reconfigurable hardware process values in fixed or floating-point formats. Minimizing bitwidths of signals carrying those values makes more parallel implementations possible and reduces power dissipation of the circuit. Arbitrary fixed-point formats are not difficult to implement and are in common use. Because of the inherent complexity of the floating-point representation, it is no less desirable, but much harder to implement arbitrary floating-point formats. This thesis presents a library of hardware modules that makes implementation of custom designs with arbitrary floating-point formats possible.

In this chapter, the reader is introduced to fixed and floating-point representations, reconfigurable hardware used to implement all the designs presented, motivation for this work and a survey of related work.